AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A compound semiconductor stacked structure having a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are successively stacked on a substrate, wherein

~~said first and second compound semiconductor layers are each a compound semiconductor layer having Sb and at least two of five elements consisting of Al, Ga, In, As and P;~~

said active layer consists of a compound semiconductor with a composition represented by $In_xGa_{1-x}As_ySb_{1-y}$ ($0.8 \leq x \leq 1.0$, $0.8 \leq y \leq 1.0$) and is thicker than 30 nm and thinner than 100 nm;

said first and second compound semiconductor layers are each a compound semiconductor layer having Sb and at least two of five elements consisting of Al, Ga, In, As and P, and [[each]] have a band gap greater than that of said active layer, and a resistance at least five times greater than that of said active layer; and

lattice constant differences between said active layer and said first and second compound semiconductor layers are set within a range of 0.1% to 1.0%. ~~0.0% to 1.2%; and~~

~~said active layer is thicker than 30 nm and thinner than 100 nm.~~

2. (Original) The compound semiconductor stacked structure as claimed n claim 1, further comprising a third compound semiconductor layer that is represented by $In_WGa_{1-W}As$ ($0 \leq w \leq 1$), and stacked on said second compound semiconductor layer.

3. (Original) The compound semiconductor stacked structure as claimed in claim 1, wherein said active layer is InAs.

4. (Previously presented) The compound semiconductor stacked structure as claimed in claim 1, wherein said first and second compound semiconductor layers are each composed of $Al_ZGa_{1-Z}As_YSb_{1-Y}$ ($0.0 \leq Z \leq 1.0$, $0.0 \leq Y \leq 0.3$).

5. (Previously presented) A magnetic sensor comprising electrodes formed on said active layer of said compound semiconductor stacked structure as defined in claim 1.

6. (Original) Mobile equipment using the magnetic sensor as defined in claim 5.

7. (Original) The mobile equipment as claimed in claim 6, wherein said mobile equipment is a mobile phone.

8. (Currently amended) A Hall device comprising:

semiconductor thin films formed on a substrate including an active layer composed of $In_{X1}Ga_{1-X1}As_{Y1}Sb_{1-Y1}$ ($0 \leq X1 \leq 1$, $0 \leq Y1 \leq 1$), and compound semiconductor layers that are formed on and under said active layer, and that have each a band gap greater than that of said active layer;

~~a metal electrode layer; and~~

a passivation covered directly a top surface and side surfaces of said semiconductor thin film other than a part of said active layer, and, ~~wherein~~

a [[said]] metal electrode layer formed on said passivation and the part on said active layer, electrically isolated from said semiconductor thin films by said passivation, and makes contact with the semiconductor thin films only with said active layer~~, and a top surface and side surfaces of said semiconductor thin films other than the contact surface are directly covered with said passivation~~.

9. (Original) The Hall device as claimed in claim 8, wherein said compound semiconductor layers are each including Sb.

10. (Original) The Hall device as claimed in claim 9, wherein the compound semiconductor layer formed on said active layer has at least two layers, and a surface layer of them is composed of $In_{X2}Ga_{1-X2}As$ ($0 \leq X2 \leq 1$).

11. (Previously presented) The Hall device as claimed in claim 8, wherein said semiconductor thin films are formed on a substrate composed of GaAs or Si, said

active layer is composed of InAs, and said compound semiconductor layers are each composed of $Al_{Z1}Ga_{1-Z1}As_{Y2}Sb_{1-Y2}$ ($0 \leq Z1 \leq 1$, $0 \leq Y2 \leq 0.3$).

12. (Cancelled).

13. (Currently amended) The [[A]] Hall device ~~comprising:~~ as claimed in claim 8, wherein a magneto-sensitive pattern with a multilayer structure that includes said [[an]] active layer formed on said substrate and composed of an $In_xGa_{1-x}As_ySb_{1-y}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$) layer greater than 30 nm and less than 100 nm in film thickness, and compound semiconductors sandwiching the active layer, wherein

input resistance R × sensitivity Vh is equal to or greater than 20 [Ω·V] under conditions that an input voltage is 1 V, and applied magnetic field is 50 mT.

14. (Original) The Hall device as claimed in claim 13, wherein said active layer has its upper and lower layers composed of Sb and at least two of five elements of Al, Ga, In, As and P.

15. (Previously presented) A pointing device using the Hall device as defined in claim 13.

16. (Previously presented) An open/close detection switch using the Hall device as defined in claim 13.

17. (Previously presented) A geomagnetic direction sensor using the Hall device as defined in claim 13.

18. (Withdrawn) A fabrication method of a Hall device comprising the steps of:

forming semiconductor thin films including an active layer composed of $In_{X1}Ga_{1-X1}As_{Y1}Sb_{1-Y1}$ ($0 \leq X1 \leq 1$, $0 \leq Y1 \leq 1$), and compound semiconductor layers that are formed on and under said active layer, and that each have a band gap greater than that of said active layer;

exposing said active layer by etching the compound semiconductor layers on regions at which a metal electrode layer is to be formed; and

forming a passivation subsequently such that it covers the entire semiconductor thin films.

19. (Withdrawn) The fabrication method of the Hall device as claimed in claim 18, further comprising the steps of:

etching said semiconductor thin films except for a magneto-sensitive pattern and electrode contact regions using the patterned passivation as a mask; and

covering with a second passivation said substrate and side surfaces of said semiconductor thin films exposed by the etching step, and said passivation.

20. (Withdrawn) The fabrication method of the Hall device as claimed in claim 18, wherein said first passivation is composed of SiO_2, and said second passivation is composed of Si_3N_4.

21. (Withdrawn) The fabrication method of the Hall device as claimed in claim 18, wherein said semiconductor thin films are formed on the substrate composed of GaAs or Si, said active layer is composed of InAs, and said compound semiconductor layers are each composed of $Al_{Z1}Ga_{1-Z1}As_{Y2}Sb_{1-Y2}$ ($0 \leq Z1 \leq 1$, $0 \leq Y2 \leq 0.3$).

22. (Withdrawn) A fabrication method of a Hall device comprising the steps of:

forming semiconductor thin films including an active layer composed of $In_{X1}Ga_{1-X1}As_{Y1}Sb_{1-Y1}$ ($0 \leq X1 \leq 1$, $0 \leq Y1 \leq 1$), and compound semiconductor layers that are formed on and under said active layer, and that each include Sb, and that each have a band gap greater than that of said active layer;

forming a first passivation after the step of forming said semiconductor thin films;

removing by etching said semiconductor thin films except for a magneto-sensitive pattern and electrode contact regions using the patterned first passivation as a mask; and

covering with a second passivation said substrate and said semiconductor thin films exposed by etching, and said first passivation.

23. (Withdrawn) The fabrication method of the Hall device as claimed in claim 22, wherein said first passivation is composed of SiO_2, and said second passivation is composed of Si_3N_4.

24. (Withdrawn) The fabrication method of the Hall device as claimed in claim 22, wherein said semiconductor thin films are formed on the substrate composed of GaAs or Si, said active layer is composed of InAs, and said compound semiconductor layers are each composed of $Al_{Z1}Ga_{1-Z1}As_{Y2}Sb_{1-Y2}$ ($0 \leq Z1 \leq 1$, $0 \leq Y2 \leq 0.3$).

25. (Withdrawn) A fabrication method of a Hall device comprising the steps of:

forming semiconductor thin films including an active layer composed of $In_{X1}Ga_{1-X1}As_{Y1}Sb_{1-Y1}$ ($0 \leq X1 \leq 1$, $0 \leq Y1 \leq 1$), and compound semiconductor layers that are formed on and under said active layer, and that each include Sb, and that each have a band gap greater than that of said active layer;

forming a first passivation after the step of forming said semiconductor thin films;

removing by etching said semiconductor thin films except for a magneto-sensitive pattern and electrode contact regions using the patterned first passivation as a mask;

exposing said active layer making contact with said metal electrode layer by removing said first passivation and upper compound semiconductor layer by etching;

covering with a second passivation said substrate and said semiconductor thin films exposed by etching, and said first passivation;

exposing said active layer by patterning said second passivation; and

forming said metal electrode layer.

26. (Withdrawn) The fabrication method of the Hall device as claimed in claim 25, wherein said first passivation is composed of SiO_2, and said second passivation is composed of Si_3N_4.

27. (Withdrawn) The fabrication method of the Hall device as claimed in claim 25, wherein said semiconductor thin films are formed on the substrate composed of GaAs or Si, said active layer is composed of InAs, and said compound semiconductor layers are each composed of $Al_{Z1}Ga_{1-Z1}As_{Y2}Sb_{1-Y2}$ ($0 \leq Z1 \leq 1$, $0 \leq Y2 \leq 0.3$).

28. (Withdrawn) A fabrication method of a Hall device comprising the steps of:

forming semiconductor thin films including an active layer composed of $In_{X1}Ga_{1-X1}As_{Y1}Sb_{1-Y1}$ ($0 \leq X1 \leq 1$, $0 \leq Y1 \leq 1$), and compound semiconductor layers that are formed on and under said active layer, and that each include Sb, and that each have a band gap greater than that of said active layer;

forming a first passivation after the step of forming said semiconductor thin films;

removing by etching said semiconductor thin films except for a magneto-sensitive pattern and electrode contact regions using the patterned first passivation as a mask; and

covering with a second passivation said substrate and said semiconductor thin films exposed by etching, and said first passivation;

exposing said active layer making contact with said metal electrode layer by removing said first and second passivation and upper compound semiconductor layer by etching;

covering said semiconductor thin films and said second passivation, which are exposed by etching, with a third passivation;

exposing said active layer by patterning said third passivation; and

forming said metal electrode layer.

29. (Withdrawn) The fabrication method of the Hall device as claimed in claim 28, wherein said first passivation is composed of SiO_2, and said second passivation is composed of Si_3N_4.

30. (Withdrawn) The fabrication method of the Hall device as claimed in claim 28, wherein said semiconductor thin films are formed on the substrate composed of GaAs or Si, said active layer is composed of InAs, and said compound semiconductor layers are each composed of $Al_{Z1}Ga_{1-Z1}As_{Y2}Sb_{1-Y2}$ ($0 \leq Z1 \leq 1$, $0 \leq Y2 \leq 0.3$).